



# Dual 1200-2500MHz Balanced Mixer with LO Buffer, IF Amp, and RF Balun

Preliminary Technical Data

**ADL5356**

## FEATURES

- RF Frequency 1200MHz to 2500MHz**
- IF Frequency 40MHz to 450MHz**
- Power Conversion Gain of 8.0dB**
- SSB Noise Figure of 10dB**
- SSB NF with +10dBm blocker of 18dB**
- Input IP3 of 26dBm**
- Input P<sub>1dB</sub> of 11 dBm**
- Typical LO Drive of 0 dBm**
- Single-ended, 50Ω RF and LO Input Ports**
- High Isolation SPDT LO Input Switch**
- Single Supply Operation: 3.3 to 5 V**
- Exposed Paddle 6 x 6 mm, 36 Lead LFCSP Package**

## APPLICATIONS

- Cellular Base Station Receivers**
- Main and Diversity Receiver Designs**
- Radio Link Downconverters**

## GENERAL DESCRIPTION

The ADL5356 utilizes two highly linear doubly balanced passive mixer cores along with integrated RF and LO balancing circuitry to enable single-ended operation. The ADL5356 incorporates two RF baluns allowing for optimal main and diversity mixer performance over a 1200 to 2500 MHz RF input frequency range using low-side LO injection for RF frequencies between 1700-2500MHz, and high-side injection for frequencies between 1200-MHz and 1700MHz. (For a high side injection version for the 1700-2500MHz band, please contact the factory). The balanced passive mixer arrangement provides good LO to RF, typically better than -36dBm, and excellent intermodulation performance. The balanced mixer cores also provide extremely high input linearity allowing the device to be used in demanding cellular applications where in-band blocking signals may otherwise result in the degradation of dynamic performance. A High linearity IF buffer amps follow the passive mixer cores, to yield a typical power conversion gain of 8.0dB, and can be utilized with a wide range of output impedances. (For a higher IIP3 version of the dual mixer without the IF amplifiers, please contact the factory).

The ADL5356 provides two switched LO paths that can be utilized in TDD applications where it is desirable to rapidly alternate between two local oscillators. LO current can be

## REV.PrE

Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties that may result from its use. Specifications subject to change without notice. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices. Trademarks and registered trademarks are the property of their respective companies.

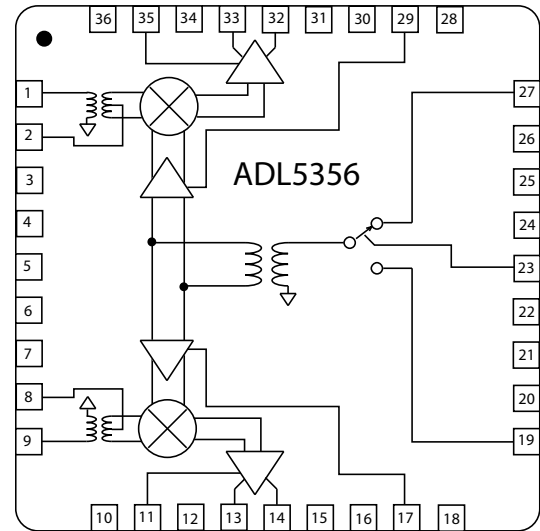


Figure 1. Functional Block Diagram

externally set using a resistor to minimize DC current commensurate with the desired level of performance. An additional 3V logic pin is provided to power down (<100uA) the circuit when desired.

For low voltage applications, the ADL5356 is capable of operation at voltages down to 3.3V with substantially reduced DC current.

The ADL5356 is fabricated using a BiCMOS high performance IC process. The device is available in a 6mm x 6mm LFCSP package and operates over a -40°C to +85°C temperature range. An evaluation board is also available.

RF Frequency	Single Mixer	Single Mixer + IF Amp	Dual Mixer + IF Amp
500MHz to 1700MHz	ADL5367	ADL5357	ADL5358
1200MHz to 2500MHz	ADL5365	ADL5355	ADL5356

ADL5356—Specifications at  $V_S=5V$ Table 1.  $V_S = 5 V$ ,  $T_A = 25^\circ C$ ,  $f_{RF} = 1900 MHz$ ,  $f_{LO} = 1697 MHz$ , LO power = 0 dBm,  $Z_o = 50\Omega$ , unless otherwise noted

Parameter	Conditions	Min	Typ	Max	Unit
<b>RF INPUT INTERFACE</b>					
Return Loss	Tunable to >20dB over a limited bandwidth		12		dB
Input Impedance			50		$\Omega$
RF Frequency Range		1200		2200	MHz
<b>OUTPUT INTERFACE</b>					
Output Impedance	Differential impedance, $f = 200 MHz$		200		$\Omega$
IF Frequency Range		40		450	MHz
DC Bias Voltage <sup>1</sup>	Externally generated		$V_S$		V
<b>LO INTERFACE</b>					
LO Power		-3	0	+10	dBm
Return Loss	Tunable to >20dB over a limited bandwidth		12		dB
Input Impedance			50		$\Omega$
LO Frequency Range	Low or High Side LO injection	1300		2200	MHz
<b>DYNAMIC PERFORMANCE</b>					
Power Conversion Gain	Including 4:1 IF port transformer and PCB loss		8.0		dB
Voltage Conversion Gain	$Z_{SOURCE} = 50\Omega$ , Differential $Z_{LOAD} = 200\Omega$ Differential		14.5		dB
SSB Noise Figure	Including 4:1 IF port transformer and PCB loss		10.0		dB
SSB Noise Figure Under-Blocking	+10dBm Blocker present +/-5MHz from wanted RF input, LO source filtered		18		dB
Input Third Order Intercept	$f_{RF1} = 1899.5 MHz$ , $f_{RF2} = 1900.5 MHz$ , $f_{LO} = 1697 MHz$ , each RF tone at -10 dBm		26.0		dBm
Input Second Order Intercept	$f_{RF1} = 1900 MHz$ , $f_{RF2} = 1850 MHz$ , $f_{LO} = 1697 MHz$ , each RF tone at -10 dBm		50		dBm
Input 1 dB Compression Point			11		dBm
LO to IF Output Leakage	Unfiltered IF Output, Improves substantially with external filter components.		-30		dBm
LO to RF Input Leakage			-45		dBm
RF to IF Output Isolation	Unfiltered IF Output		45		dBc
RFI1 to RFI2 Channel Isolation			45		
IF/2 Spurious	-10 dBm Input Power		-65		dBc
IF/3 Spurious	-10 dBm Input Power		-75		dBc
<b>POWER INTERFACE</b>					
Supply Voltage		3.3	5	5.5	V
Quiescent Current	Resistor Programmable		360		mA

<sup>1</sup> Supply voltage must be applied from external circuit through external inductors.

**ADL5356—Specifications at  $V_S=3.3V$** **Table 2.**  $V_S = 3.3 V$ ,  $T_A = 25^\circ C$ ,  $f_{RF} = 1900 MHz$ ,  $f_{LO} = 1697 MHz$ , LO power = 0 dBm,  $Z_o = 50\Omega$ , unless otherwise noted

Parameter	Conditions	Min	Typ	Max	Unit
<b>DYNAMIC PERFORMANCE</b>					
Power Conversion Gain	Including 4:1 IF port transformer and PCB loss		8.7		dB
Voltage Conversion Gain	$Z_{SOURCE} = 50\Omega$ , Differential $Z_{LOAD} = 200\Omega$ Differential		15.2		dB
SSB Noise Figure	Including 4:1 IF port transformer and PCB loss		9.0		dB
Input Third Order Intercept	$f_{RF1} = 1899.5 MHz$ , $f_{RF2} = 1900.5 MHz$ , $f_{LO} = 1697 MHz$ , each RF tone at -10 dBm		20		dBm
Input Second Order Intercept	$f_{RF1} = 1900 MHz$ , $f_{RF2} = 1850 MHz$ , $f_{LO} = 1697 MHz$ , each RF tone at -10 dBm		50		dBm
Input 1 dB Compression Point			7		dBm
<b>POWER INTERFACE</b>					
Supply Voltage		3.0	3.3	3.6	V
Quiescent Current	Resistor Programmable		265		mA

## ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage, $V_{POS}$	5.5 V
PWDN, LOSW, VGS0, VGS1, VGS2	3.3 V
RF Input Power, DVIN, MNIN	TBD
Internal Power Dissipation	TBD
$\theta_{JA}$ (Exposed Paddle Soldered Down)	TBD
$\theta_{JC}$ (At Exposed Paddle)	TBD
Maximum Junction Temperature	TBD
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### ESD CAUTION



#### ESD (electrostatic discharge) sensitive device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

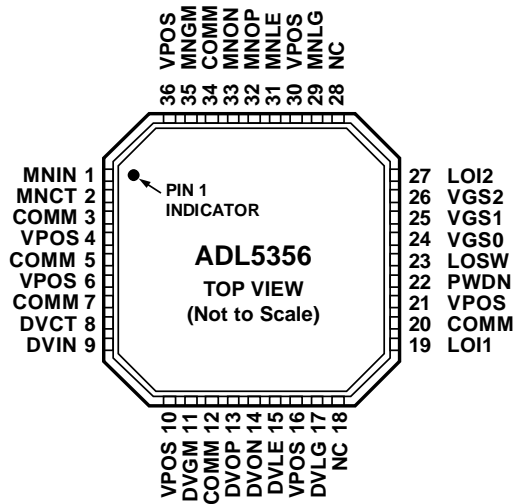


Figure 2. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Function
1	MNIN	RF Input for Main Channel. Internally matched to 50Ω. Must be ac-coupled.
2	MNCT	Center Tap for Main Channel Input Balun. Should be bypassed to ground using low inductance capacitor.
3, 5, 7, 12, 20, 34	COMM	Device Common (DC Ground).
4, 6, 10, 16, 21, 30, 36	VPOS	Positive Supply Voltage.
8	DVCT	Center Tap for Diversity Channel Input Balun. Should be bypassed to ground using low inductance capacitor.
9	DVIN	RF Input for Diversity Channel. Internally matched to 50Ω. Must be ac-coupled.
11	DVGM	Diversity Amplifier Bias Setting. Connect 1.2kΩ resistor to ground for typical operation.
13, 14	DVOP, DVON	Diversity Channel Differential Open-Collector Outputs. DVOP and DVON should be pulled-up to VCC using external inductors.
15	DVLE	Diversity Channel External Inductor. Connect 10nH inductor to ground for typical operation.
17	DVLG	Diversity Channel LO Buffer Bias Setting. Connect 390Ω resistor to ground for typical operation.
18, 28	NC	No Connect.
19,	LOI1	Local Oscillator Input 1. Internally matched to 50Ω. Must be ac-coupled.
22	PWDN	Connect to Ground for Normal Operation. Connect pin to 3.3V for disable mode.
23	LOSW	Local Oscillator Input Selection Switch. Set LOSW high to select LOI1, and set low to select LOI2.
24, 25, 26	VGS0, VGS1, VGS2	Gate to Source Control Voltages. For typical operation set VGS2 high and VGS0 and VGS1 to low logic level.
27	LOI2	Local Oscillator Input 2. Internally matched to 50Ω. Must be ac-coupled.
29	MNLG	Main Channel LO Buffer Bias Setting. Connect 390Ω resistor to ground for typical operation.
31	MNLE	Main Channel External Inductor. Connect 10nH inductor to ground for typical operation.
32, 33	MNOP, MNON	Main Channel Differential Open-Collector Outputs. MNOP and MNON should be pulled-up to VCC using external inductors.
35	MNGM	Main Amplifier Bias Setting. Connect 1.2kΩ resistor to ground for typical operation.

TYPICAL PERFORMANCE CHARACTERISTICS—PRELIMINARY DATA

$V_S = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ , as measured using typical circuit schematic with low-side LO unless otherwise noted.

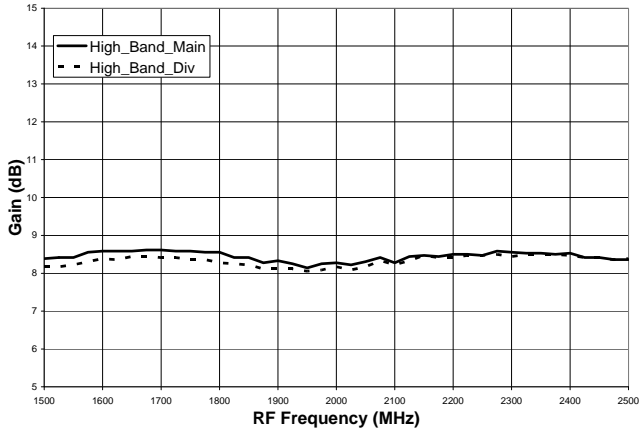


Figure 3. Conversion Gain versus RF Frequency

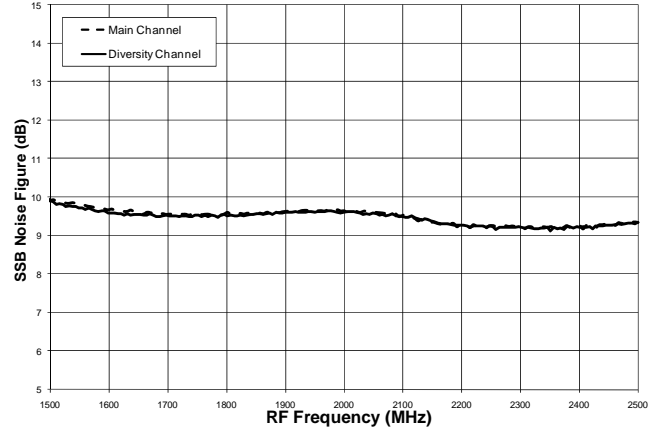


Figure 6. Single-Sideband NF versus RF Frequency

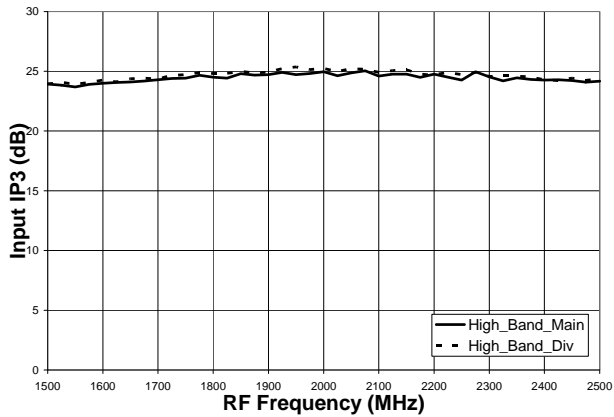


Figure 4. IIP3 versus RF Frequency

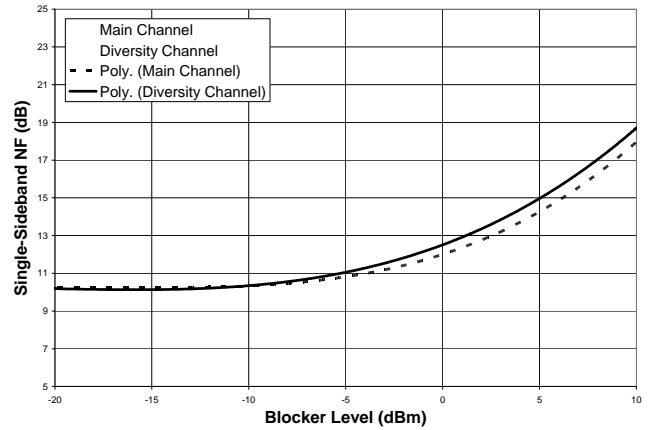


Figure 7. Single-Sideband NF versus Blocker Level at 1950MHz

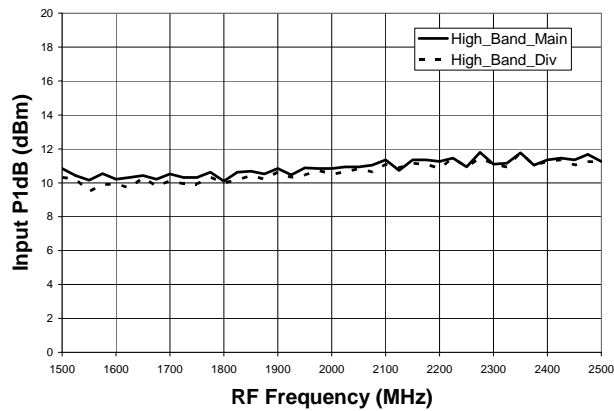


Figure 5. IP1dB versus RF Frequency

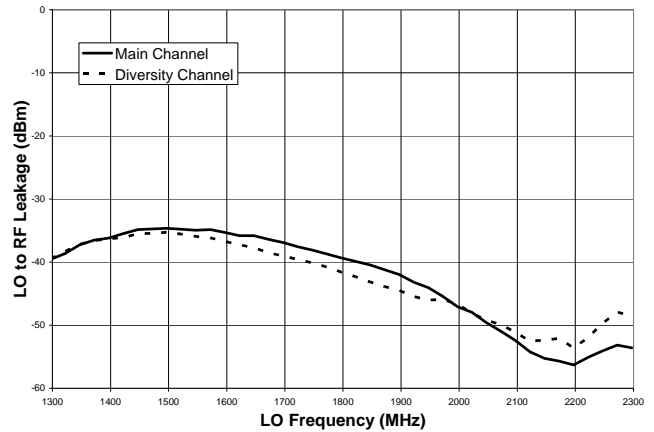


Figure 8. LO to RF Leakage versus LO Frequency

# TYPICAL PERFORMANCE CHARACTERISTICS—PRELIMINARY DATA

$V_S = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ , as measured using typical circuit schematic with low-side LO unless otherwise noted.

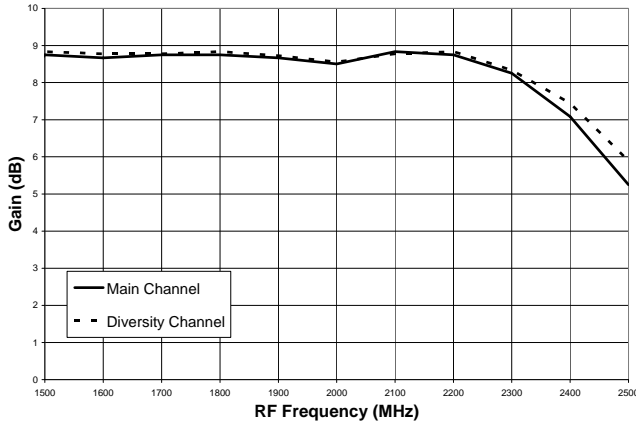


Figure 9. Conversion Gain versus RF Frequency

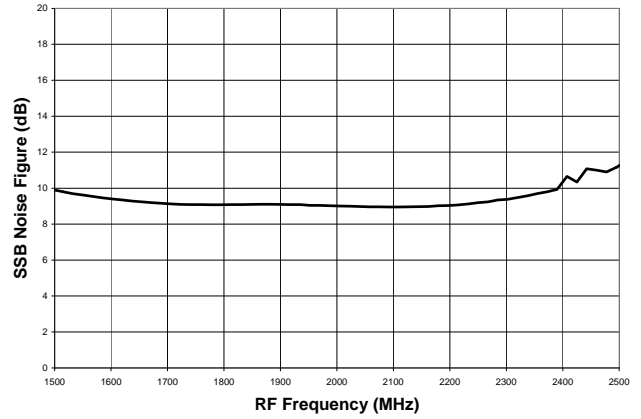


Figure 12. Single-Sideband NF versus RF Frequency

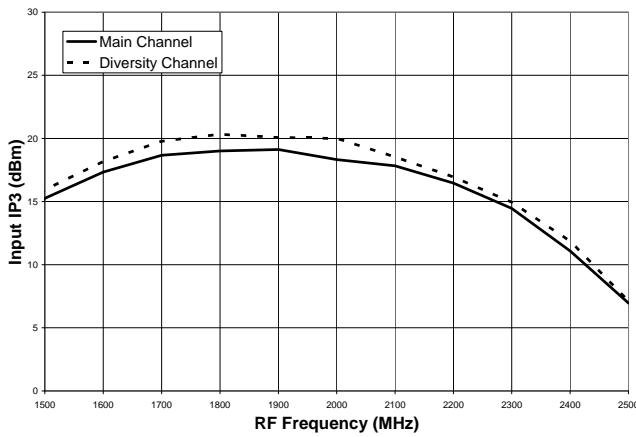


Figure 10. IIP3 versus RF Frequency

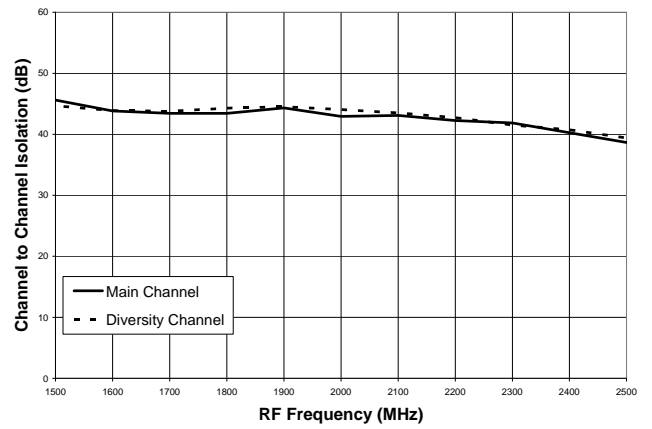


Figure 13. Channel to Channel Isolation vs. RF Frequency

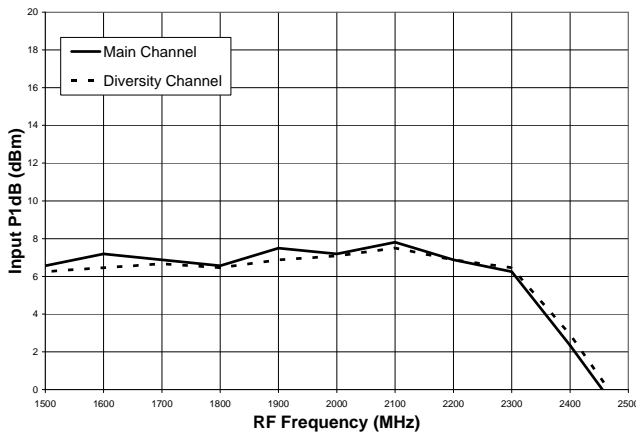


Figure 11. IP1dB versus RF Frequency

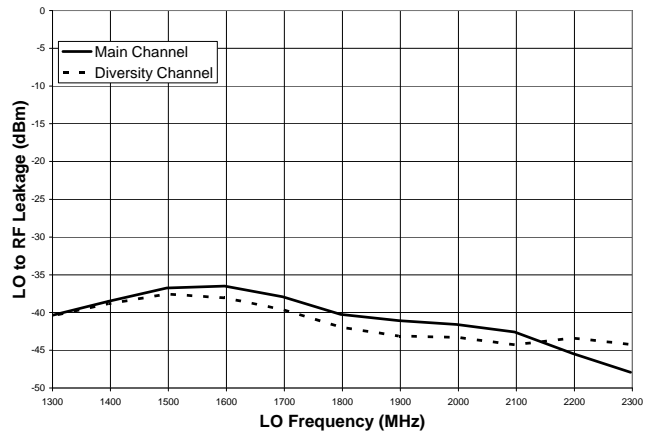


Figure 14. LO to RF Leakage versus LO Frequency

EVALUATION BOARD SCHEMATIC

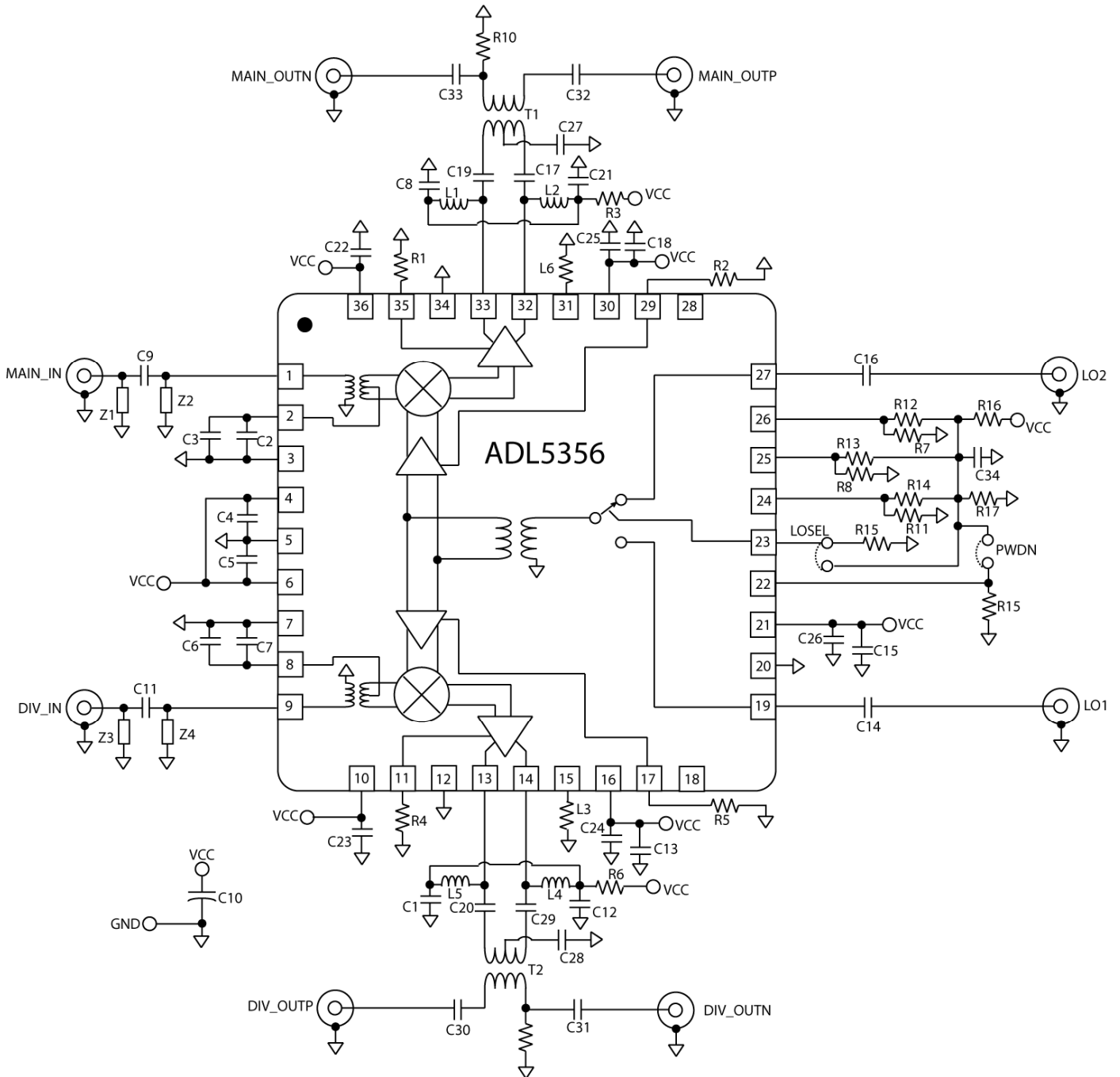


Figure 9. Evaluation Board Schematic.

Table 3. Eval Board Configuration

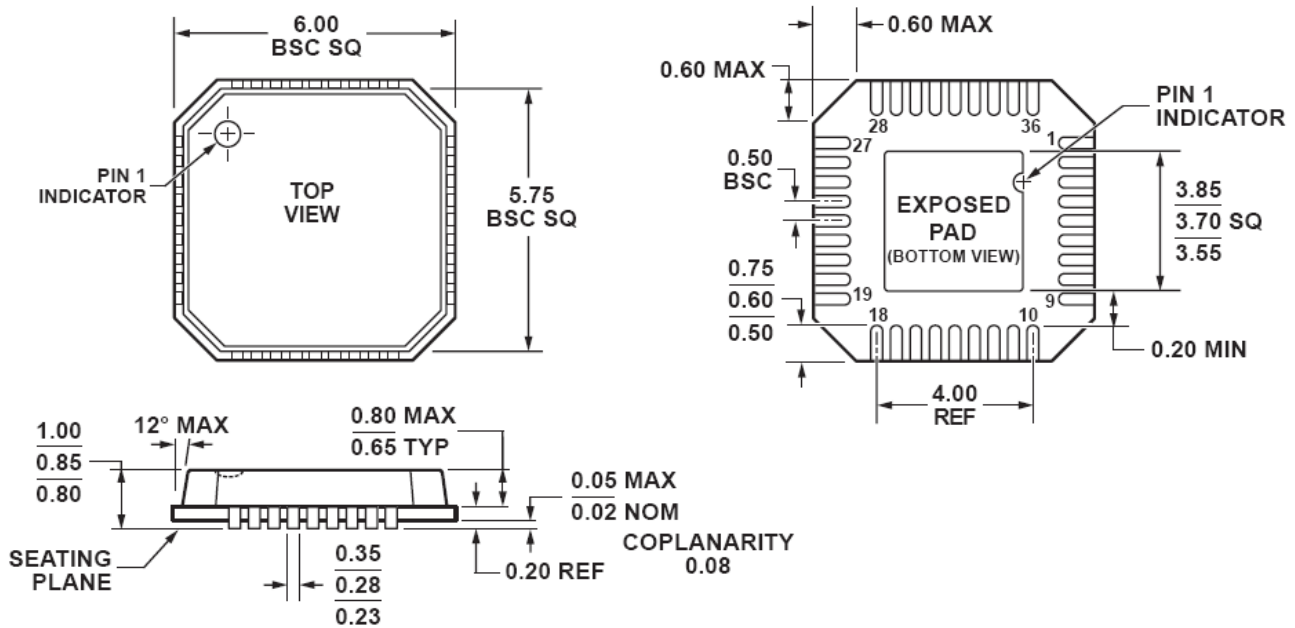


Components	Function	Default Conditions
C1, C4, C5, C8, C10, C12, C13, C15, C18, C21, C22, C23, C24, C25, C26	Power Supply Decoupling. Nominal supply decoupling consists a 0.01 $\mu$ F capacitor to ground in parallel with 10pF capacitors to ground positioned as close to the device as possible.	C10 = 4.7 $\mu$ F (size 3216) C1, C8, C12, C21 = 150pF (size 0402) C4, C5, C22, C23, C24, C25, C26 = 10pF (size 0402) C13, C15, C18 = 0.1 $\mu$ (size 0402)
Z1-Z4, C2, C3, C6, C7, C9, C22	RF Main and Diversity Input Interface. Main and Diversity input channels are ac-coupled through C9 and C22. Z1-Z4 provides additional component placement for external matching/filter networks. C2, C3, C6, and C7 provide bypassing for the center taps of the main and diversity on-chip input baluns.	C2, C7 = 10pF (size 0402) C3, C6 = 0.01 $\mu$ F (size 0402) C9, C22 = 22pF (size 0402) Z1-Z4 = open (size 0402)
T1, T2, C17, C19, C20, C27, C28, C29, C30, C31, C32, C33, L1, L2, L4, L5, R3, R6, R9, R10	IF Main and Diversity Output Interface. The open collector IF output interfaces are biased through pull-up choke inductors L1, L2, L4, and L5, with R3 and R6 available for additional supply bypassing. T1 and T2 are 4:1 impedance transformers used to provide a single ended IF output interface, with C27 and C28 providing center-tap bypassing. C17, C19, C20, C29, C30, C31, C32, and C33 ensure an ac-coupled output interface. R9 and R10 should be removed for balanced output operation.	C17, C19, C20, C29-C33 = 0.001 $\mu$ F (size 0402) C27, C28 = 150pF (size 0402) T1, T2 = TC4-1T+ (MiniCircuits) L1, L2, L4, L5 = 330 nH (size 0805) R3, R6, R9, R10 = 0 $\Omega$ (size 0402)
C14, C16, R15, LOSEL	LO Interface. C14 and C16 provide ac-coupling for the LOI1 and LOI2 local oscillator inputs. LOSEL selects the appropriate LO input for both mixer cores. R15 provides a pull-down to ensure LOI2 is enabled when the LOSEL jumper is removed. Jumper can be removed to allow LOSEL interface to be exercised using external logic generator.	C14, C16 = 10pF (size 0402) R15 = 10k $\Omega$ (size 0402) LOSEL = 2-pin shunt
R19, PWDN	PWDN Interface. When the PWDN 2-pin shunt is inserted the ADL5356 is powered down. When open R19 pulls the PWDN logic low and enables the device. Jumper can be removed to allow PWDN interface to be exercised using external logic generator. It is permissible to ground the pwrnd pin for nominal operation.	R19 = 10k $\Omega$ (size 0402) PWDN = 2-pin shunt
R1, R2, R4, R5, L3, L6, R7, R8, R11, R12, R13, R14, R16, R17, C34	Bias Control. R16 and R17 form a voltage divider to provide a 3V for logic control, bypassed to ground through C34. R7, R8, R11, R12, R13, and R14 provide resistor programmability of VGS0, VGS1 and VGS2. Typically these nodes can be hard-wired for nominal operation. It is permissible to ground these pins for nominal operation. R2 and R5 set the bias point for the internal LO buffers. R1 and R4 set the bias point for the internal IF amplifiers. L3 and L6 are external inductors used to improve isolation and common mode rejection.	R1, R4 = 1.54k $\Omega$ (size 0402) R2, R5 = 390 $\Omega$ (size 0402) L3, L6 = 0 $\Omega$ (size 0603) R12, R13, R14 = open (size 0402) R7, R8, R11 = 0 $\Omega$ (size 0402) R16 = 10k $\Omega$ (size 0402) R17 = 15k $\Omega$ (size 0402) C34 = 1nF (size 0402)

## OUTLINE DIMENSIONS



36-Lead Lead Frame Chip Scale Package [LFCSP\_VQ]  
 6 x 6 mm Body, Very Thin Quad  
 (CP-36-1)  
 Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220-VJJD-1

Figure 10. 36-Lead Lead Frame Chip Scale Package [LFCSP\_VQ]  
 6mm x 6 mm Body, Very Thin Quad (CP-36-1)  
 Dimensions shown in millimeters

050808-D

## ORDERING GUIDE

Models	Temperature Range	Package Description	Package Option	Branding	Transport Media Quantity
ADL5356XCPZ-R7	-40°C to +85°C	36-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-36-1	TBD	TBD, Reel
ADL5356XCPZ-WP	-40°C to +85°C	36-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-36-1	TBD	TBD, Waffle Pack
ADL5356-EVALZ		Evaluation Board			1